REMARKS

The Examiner has again pending Claims 1, 2, 4-16 and 18 under 35 USC § 103 as unpatentable over the teachings of the Cameron patent in view of the admitted prior art (AAPA) regarding the AIX technology. In addition, the Examiner has rejected Claims 3 and 17 under 35 USC § 103 as unpatentable over the teachings of the Cameron patent in view of the AAPA and the teachings of the Ripps reference. Finally, the Examiner has rejected Claims 1 and 11 as unpatentable over Zolnowsky in view of Custer and the AAPA; or, alternatively, as unpatentable over Boland in view of Custer and the AAPA.

As previously argued, and as agreed to by the Examiner, the Cameron patent is directed to the scheduling of tasks across multiple nodes (with node defined at Column 2, line 40 as a single processor location) wherein, as specifically stated in Column 2, lines 53-58 and again at Column 7, lines 37-42, "...only one application program is active at a time on any one node and an entire application program is active at once across all of the nodes on which the application program is loaded." While the Cameron patent does state that more than one application program may be loaded on a single node, it clearly requires that only one application

be active at any time on that node, and therefore that global scheduling is a trivial task. The Examiner has commented that the previously-examined language of independent Claims 1 and 11 did not explicitly recite that the multiple tasks of more than one application could be executed at the same time. Therefore, the language of independent Claims 1 and 11, and therefore also of all of the remaining claims which depend therefrom, has been amended to additionally recite that limitation which is clearly not taught or suggested by the combination of references of Cameron, the AAPA and Ripps.

The Examiner has cited the Zolnowsky patent in combination with the teachings of Custer and of the AAPA in rejecting Claims 1 and 11. The Zolnowsky patent discloses a system wherein there is one scheduler for each one processor, each of which has an associated dispatch queue. In the Zolnowsky system, a processor can select a thread from and place a thread on a global queue, its own queue, or another processor's queue. When a processor selects a thread, it performs a synchronization algorithm to ensure that another processor does not also select that thread. Applicants respectfully submit that the Zolnowsky teachings,

alone or in combination with the Custer and AAPA teachings, do not obviate the invention as claimed.

It is first to be noted that the Zolnowsky does not teach a scheduler means for creating a prioritized schedule of tasks of more than one application. The Zolnowsky system has a "high priority real time queue" on which any of the processors can place a thread (see: column 7, lines 43-48). It cannot be maintained, therefore, that the high priority real time queue is a scheduler means which dynamically creates a prioritized schedule which is then used by local schedulers. In addition, the Zolnowsky patent does not provide at least one local scheduler associated with each the more than one computing nodes which each have a plurality of processes. In Zolnowsky, there is one scheduler per processor. Furthermore, the schedulers (i.e., the one scheduler per processor) do not adhere to a prioritized schedule obtained from a global scheduler, but rather "...determine when and which threads are to be dispatched for execution on the system processors" (see: column 7, lines 15-20) in accordance with a protocol which is schematically illustrated in Zolnowsky's Figure 8.

The Examiner has cited Custer page 84 as teaching the combining of a thread with a process. The Examiner further avers that the Zolnowsky dispatching of threads together with the Custer combining of threads to processes obviates the means for "ascertaining which process(es) are assigned to the tasks". It is respectfully asserted that the Custer disclosure regarding threads and processes does not teach or suggest ascertaining which tasks are to be assigned to which processes by a local scheduler in implementing a prioritized schedule from a global scheduler. Even if one were to combine the teachings of Zolnowsky and Custer, one would not arrive at the invention as claimed. In combining Zolnowsky and Custer, one would simply have the scheduler which is associated with the one processor identifying which entity within the process is to execute. Custer does not supply any teachings which would modify Zolnowsky to provide for ascertaining which tasks are assigned to which processes and further for prioritizing in accordance with a global prioritization schedule.

The Examiner goes on to acknowledge that the combination of Zolnowsky and Custer would not teach means for prioritizing the processes according to the prioritized

schedule. Applicants respectfully contend that the AAPA would not logically be combined with Zolnowsky and Custer, and further that any such combination would not yield the invention as presently claimed. It is herein reiterated that the AIX teachings from the AAPA relate to a system wherein only one application is active at a time and wherein the assignment of priorities of processes is simply a resource utilization mechanism. There is no suggestion in the AIX prior art that process priorities would or could be used for the purpose of anticipatory scheduling of multiple tasks of different applications to be executed simultaneously. The only applicability of the AAPA teachings to the Zolnowsky system would be to replace the Figure 8 protocol, which one of ordinary skill in the art would not be inclined to do because it would limit the functioning of the Zolnowsky scheduler.

The Examiner has additionally rejected Claims 1 and 11 as unpatentable over the combined teachings of Boland, Custer and AAPA. The Boland patent is directed to the scheduling of processes when a process has affinity (based on previous running of that process) with a particular processor. Under the Boland system, the highest priority

"affinitized" process is scheduled before the highest priority "non-affinitized" process. There are no teachings in the Boland patent of a scheduler means for dynamically creating a prioritized schedule, nor of local schedulers for ascertaining assignment of tasks to processes and for prioritizing the assigned processes in accordance with the prioritized schedule. In Boland, the scheduler 22 enters processes into the global run queue 24 which may thereafter be reordered (though by what entity, Boland does not say) in the global priority run queue 26 with priority levels and FIFO scheduling within the levels (see: column 4, lines 16-26). There is no local scheduling entity taught or suggested by Boland. Applicants disagree with the Examiner's statement that each Boland processors' consulting with the global priority queue (as mentioned at column 4, line 28 of Boland) inherently requires a local scheduler to analyze the queue. There is no teaching of a local scheduler. Boland simply teaches that the processor consults (i.e., looks at) the queue to see what it should do next. There is nothing in Boland that teaches or suggests that the processor has the capability to do anything other than read from the "top" of the queue. Applicants aver that

the Examiner cannot rely on "inherency" to supply teachings which are clearly not found in the cited reference. Since neither of the additionally cited Custer or AAPA references teach global and local schedulers, it cannot be maintained that the invention as claimed is obviated by the combined teachings.

In light of the foregoing arguments, it is respectfully requested that the rejections based on the combined teachings of the Cameron patent and AIX material, the Zolnowsky, Custer and AAPA references, or the Boland, Custer and AAPA references, be withdrawn. Applicants request reconsideration of the claims as amended.

Respectfully submitted,

M.A. COHEN, ET AL

By: Anne Vachon Dougherty

Anne Vachon Dougherty
Registration No. 30,374
Tel. (914) 962-5910